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For

METHOD OF FABRICATING SEMICONDUCTOR DEVICE HAVING TRIPLE LDD STRUCTURE AND LOWER GATE RESISTANCE FORMED WITH A SINGLE IMPLANT PROCESS

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METHOD OF FABRICATING SEMICONDUCTOR DEVICE HAVING TRIPLE LDD STRUCTURE AND LOWER GATE RESISTANCE FORMED WITH A SINGLE IMPLANT PROCESS

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention generally relates to semiconductor fabrication processes. More particularly, the present invention relates to the field of fabricating semiconductor devices having a triple LDD (lateral diffused dopants) structure.

RELATED ART

Semiconductor fabrication processes have made possible the fabrication of advanced integrated circuits on a semiconductor wafer. These semiconductor fabrication processes are complex, requiring extensive control and care to avoid fabricating defective integrated circuits.

Due to the need for high speed and low-voltage, advanced structures have been developed for semiconductor devices such as MOSFETs (metal oxide semiconductor field effect transistor). One such structure is the triple LDD (lateral diffused dopants) structure for the source and drain of the MOSFET. In particular, the triple LDD structure provides a solution to short channel effects.

Figures 1A-1F illustrate a conventional method of fabricating a semiconductor device having a triple LDD (lateral diffused dopants) structure. Here, the semiconductor device is a MOSFET 100. As shown in Figure 1A, a gate structure 10 is formed on the surface of a semiconductor substrate 40. Then, a first implant process is performed to implant a dopant into the semiconductor substrate 40 to form a source 20 and a drain 30. Here, the source 20 and the drain 30 have a single LDD structure.

Moreover, Figure 1B shows that a first spacer 50 is formed adjacent to the vertical surfaces of the gate structure 10. Furthermore, a second implant process is performed to implant a dopant into the semiconductor substrate 40 to further define the source 20 and the drain 30, as depicted in Figure 1C. Here, the source 20 and the drain 30 have a double LDD structure.

Additionally, Figure 1D shows that a second spacer 60 is formed adjacent to the vertical surfaces of the gate structure 10. A third implant process is performed to implant a dopant into the semiconductor substrate 40 to further define the source 20 and the drain 30, as depicted in Figure 1E. Here, the source 20 and the drain 30 finally have the triple LDD structure.

Furthermore, a silicidation process is performed to form a silicide 70 on the horizontal surface of the gate structure 10 and on the surface of the source 10 and the drain 10 as shown in Figure 1F, whereas the silicide 70 is used as a contact.

As illustrated in Figures 1A-1F, this conventional fabrication method requires three separate implant processes. Each implant process is costly and time consuming. Moreover, the first and second spacers 50 and 60 cover portions of the surface area of the gate structure 10, reducing the surface area of the gate structure 10 that is available for the silicide 70 to be formed. This can lead to higher gate resistance as the width of the gate structure 10 is decreased in advanced semiconductor fabrication applications.

SUMMARY OF THE INVENTION

A method of fabricating a semiconductor device having a triple LDD (lateral diffused dopants) structure is disclosed. This fabrication method requires a single implant process, leading to reduction in fabrication costs and fabrication time. Moreover, this fabrication method increases the surface area of the gate structure of the semiconductor device that is available for silicide to be formed, leading to lower gate resistance. In an embodiment, the method of fabricating the semiconductor device having the triple LDD (lateral diffused dopants) structure comprises forming a gate structure on a surface of a semiconductor substrate. The gate structure includes a first vertical surface and a second vertical surface. Then, a first spacer adjacent to the first vertical surface and a second spacer adjacent to the second vertical surface are formed. The first spacer has a first thickness and a second thickness that is greater than the first thickness and that abuts the first vertical surface. The second spacer has a third thickness and a fourth thickness that is greater than the third thickness and that abuts the second vertical surface. Moreover, a single implant process is performed to form the triple LDD structure for a drain and a source of the semiconductor device in the semiconductor substrate.

These and other advantages of the present invention will no doubt become apparent to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments, which are illustrated in the drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the present invention.

Figures 1A-1F illustrate a conventional method of fabricating a semiconductor device having a triple LDD (lateral diffused dopants) structure.

Figures 2A-2H illustrate a method of fabricating a semiconductor device having a triple LDD (lateral diffused dopants) structure in accordance with an embodiment of the present invention.

The drawings referred to in this description should not be understood as being drawn to scale except if specifically noted.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention.

A method of fabricating a semiconductor device having a triple LDD (lateral diffused dopants) structure is disclosed. This fabrication method requires a single implant process, leading to reduction in fabrication costs and fabrication time. Moreover, this fabrication method increases the surface area of the gate structure of the semiconductor device that is available for silicide to be formed, leading to lower gate resistance.

Figures 2A-2H illustrate a method of fabricating a semiconductor device having a triple LDD (lateral diffused dopants) structure in accordance with an embodiment of the present invention. In an embodiment, the semiconductor device is a MOSFET (metal oxide semiconductor field effect transistor) 200.

As depicted in Figure 2A, a gate structure 210 is formed on the surface of a semiconductor substrate 240. In an embodiment, the gate structure 210 includes a gate 210A comprised of polysilicon and a gate oxide 210B comprised of silicon dioxide. Furthermore, a first mask M1 is deposited on the surface of the semiconductor substrate 240 and on the gate structure 210, as shown in Figure 2B. The first mask M1 can be deposited using any deposition process such as chemical vapor deposition.

A second mask M2 is deposited on the surface of the semiconductor substrate 240 and on the gate structure 210, as shown in Figure 2C. The second mask M2 can be deposited using any deposition process such as chemical vapor deposition.

As shown in Figure 2D, a first plasma etch process is performed to remove substantially the second mask M2, whereas the first plasma etch process is an anisotropic etch. The first plasma etch process uses a first plasma that has a first etch rate with respect to the first mask M1 and a second etch rate with respect to the second mask M2. Here, the second etch rate is substantially greater than the first etch rate, enabling substantial removal of the second mask M2 without removing a significant portion of the first mask M1. Since the second mask M2 is thicker at the corners 285 and 286 (of

Figure 2C) and since the first plasma etch process is an anisotropic etch, the portion of the second mask M2 that remains after performing the first plasma etch process is located in the corners 285 and 286 (of Figure 2C).

Furthermore, a second plasma etch process is performed to remove substantially the first mask M1, as depicted in Figure 2E. The second plasma etch process is an anisotropic etch. The second plasma etch process uses a second plasma that has a first etch rate with respect to the first mask M1, a second etch rate with respect to the second mask M2, and a third etch rate with respect to the gate structure 210. Here, the first etch rate is substantially greater than the second etch rate and the third etch rate, enabling substantial removal of the first mask M1 without completely removing the second mask M2 and without removing a significant portion of the gate structure 210. Since the second mask M2 covers the first mask M1 at the corners 295 and 296 (of Figure 2D), since the second plasma etch process is an anisotropic etch, and since first etch rate of the second plasma etch process is substantially greater than the second etch rate of the second plasma etch process and the third etch rate of the second plasma etch process, the portion of the first mask M1 that remains after performing the second plasma etch process is located in the corners 295 and 986 (of Figure 2D).

Moreover, a third plasma etch process is performed to remove completely the second mask M2, as depicted in Figure 2F. The third plasma etch process uses a third plasma that has a first etch rate with respect to the first mask M1, a second etch rate with respect to the second mask M2, and a third etch rate with respect to the gate structure 210. Here, the second etch rate is substantially greater than the first etch rate and the third etch rate, enabling complete removal of the second mask M2 without completely removing the first mask M1 and without removing a significant portion of the gate structure 210. The remaining portions of the first mask M1 form and define a first spacer 260 and a second spacer 261.

The first spacer 260 is formed adjacent to a first vertical surface of the gate structure 210. The second spacer 261 is formed adjacent to a second vertical surface of the gate structure 210. The first spacer 260 has a first thickness and a second thickness that is greater than the first thickness and that abuts the first vertical surface of the gate structure 210. Additionally, the second spacer 261 has a third thickness and a fourth thickness that is greater than the third thickness and that abuts the second vertical surface of the gate structure 210.

In an embodiment, the first mask M1 is silicon nitride while the second mask M2 is silicon dioxide. It should be understood that the first mask M1 and the second mask M2 can be other materials.

As depicted in Figure 2G, a single implant process is performed to implant a dopant into the semiconductor substrate 240 to form the triple LDD structure for the source 220 and the drain 230 of the MOSFET 200. In an embodiment, the implant process is an ion implant process. The multiple thicknesses of the first spacer 260 and the second spacer 261 control the dopant penetration into the semiconductor substrate 240, providing the triple LDD structure for the source 220 and drain 230 of the MOSFET 200. During the implant process, the thickest portions of the first and second spacers 260 and 261 severely limit the dopant penetration into the semiconductor substrate 240 while the other portions of the first and second spacers 260 and 261 less severely limit the dopant penetration into the semiconductor substrate 240. The greatest penetration into the semiconductor substrate 240 is achieved where there is no spacer or gate structure 210 on the surface of the semiconductor substrate 240. Since a single implant process is performed, reduction in fabrication costs and fabrication time are achieved.

In an n-type MOSFET, the source 220 and drain 230 are doped with an n-type dopant. In a p-type MOSFET, the source 220 and drain 230 are doped with a p-type dopant.

Moreover, Figure 2G shows that an upper portion 201 of the first vertical surface of the gate structure 210 and an upper portion 202 of the second vertical surface of the gate structure 210 are available for formation of a silicide during a silicidation process, increasing the surface area on the gate structure 210 for the silicide. This increased surface area on the gate structure 210 for the silicide leads to a lower gate resistance even if the width of the gate structure 210 is reduced.

Furthermore, a silicidation process is performed as shown in Figure 2H. A metal such as cobalt, nickel, aluminum, or titanium is utilized in the silicidation process. The silicidation process causes the formation of a first silicide 270B on the source 220 and the formation of a second silicide 270C on the drain 230, whereas the first silicide 270B and the second silicide 270C act as contacts. Moreover, the silicidation process causes formation of a third silicide 270A on the horizontal surface of the gate structure 210, on an upper portion 201 (Figure 2G) of the first vertical surface of the gate structure 210, and on an upper portion 202 (Figure 2G) of the second vertical surface of the gate structure 210.

The MOSFET 200 exhibits a lower gate resistance compared to the MOSFET 100 of the prior art since the MOSFET 200 has a greater surface area for supporting silicidation. This provides improved performance relative to the MOSFET 100 of the prior art.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications and variations are possible

in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.